GENERAL INSTRUMENT

RO-3-9503

Graphics ROM

FEATURES

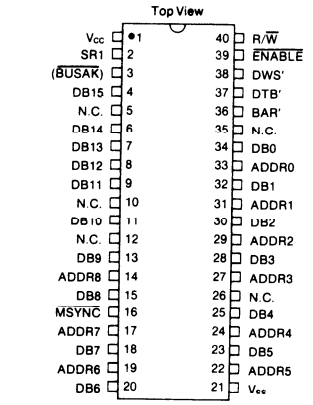
- Mask programable storage providing 2048 x 8 bit words
- 16 bit on-chip address latch
- Memory map circuitry to place the 2K ROM page within a 65K memory area
- 8 bit tri-state bus with higher 8 bits driven to zero during read operations
- 11 bit, static address outputs for external memory
- Control signals for external memory:
  $\overline{\text{ENABLE}}$
  R/$\overline{\text{W}}$
- Bus drive capability, 1 TTL load and 100pf plus tri-state

OPERATING DESCRIPTION

The device operates in three memory configurations. These configurations are selected via the input control signals.

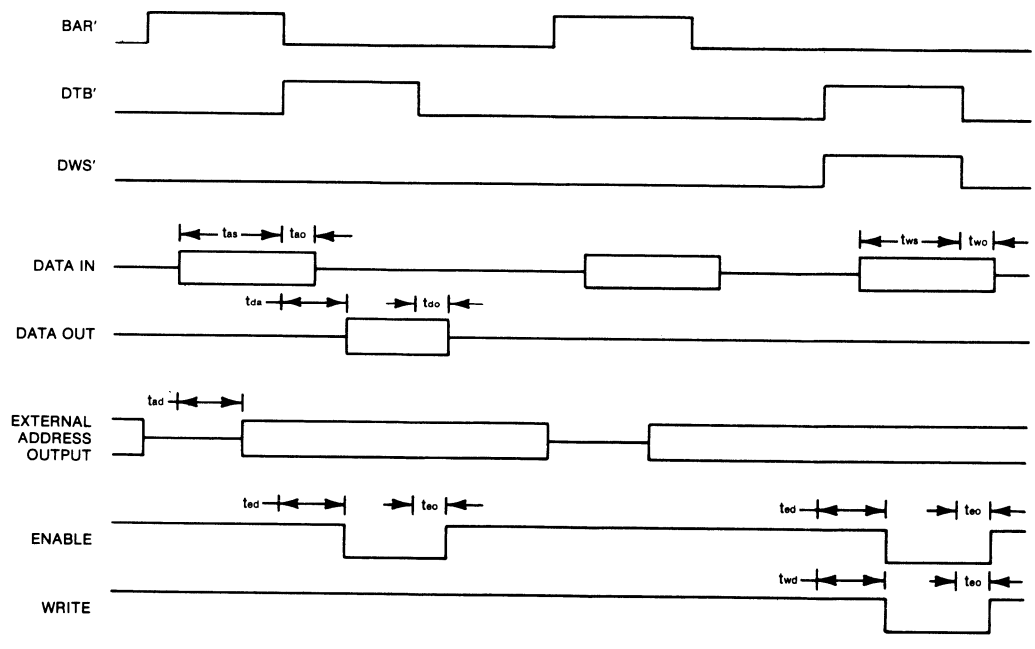
1. When SR1 has been pulsed negative, the memory is located at 12288 to 14335. The external memory is addressed at 14336 to 16383.
2. When $\overline{\text{BUSAK}}$ has been pulsed negative, the memory is located at 0 to 2047. The external memory is addressed at 2048 to 4095.
3. When BAR' and DWS' are pulsed positive, the memory will not respond to address bit 9 and address bit 10, which restricts the memory to 512 locations. The memory is now located from 0 to 511 relative to the current memory origin. The external memory is also addressable from 0 to 511 relative to its current origin. Configuration three may be released by applying a negative pulse on the SR1 input.

PIN CONFIGURATION
40 LEAD DUAL IN LINE

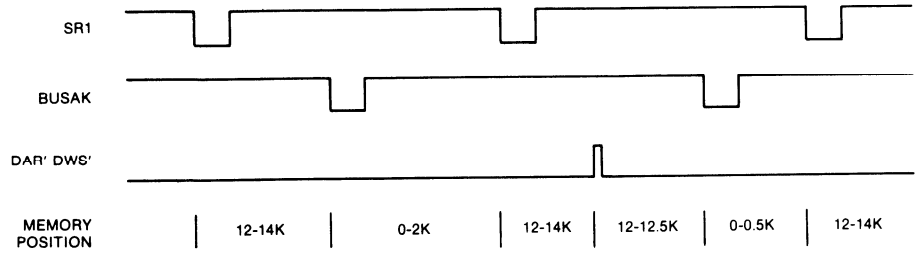


VIDEO

MEMORY TIMING



MEMORY POSITION RELATIVE TO CONTROL OPERATION



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Temperature Under Bias ..... 0° C to +40° C
Storage Temperature ..... −55° C to +150° C
All Input or Output Voltages with Respect to V_{SS} ..... −0.2V to +9.0V
V_{CC} with Respect to V_{SS} ..... −0.2V to +9.0V

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Standard Conditions (unless otherwise noted)

T_A = 0° C to +40° C
V_{CC} = +4.85V − + 5.15V
V_{SS} = 0.0V

Characteristic	Sym	Min	Typ	Max	Units	Conditions
DC CHARACTERISTICS						
Bus Inputs						
Input Logic Low	V_{IL}	0	—	0.7	Volts	
Input Logic High	V_{IH}	2.4	—	V_{CC}	Volts	
Input Leakage	I_{IL}	—	—	10	μA	$V_{IN} = V_{CC}$
CPU BUS Outputs						
Output Logic Low	V_{OL}	0	—	0.5	Volts	1 TTL Load
Output Logic High	V_{OH}	2.4	—	V_{CC}	Volts	+100pF
Address and Enable Outputs						
Output Logic Low	V_{OL}	0	—	0.5	Volts	1 TTL Load
Output Logic High	V_{OH}	2.4	—	V_{CC}	Volts	+100pF
Supply Current						
V_{CC} Current	I_{CC}	—	—	150	mA	V_{CC} = +5.25V @ 40° C
AC CHARACTERISTICS						
Bus Inputs						
Address Set Up	t_{as}	300	—	—	ns	
Address Overlap	t_{ao}	—	50	—	ns	
Write Set Up	t_{ws}	300	—	—	ns	
Write Overlap	t_{wo}	—	50	—	ns	
CPU BUS Outputs						
Turn ON Delay	t_{da}	—	—	300	ns	1 TTL Load
Turn OFF Delay	t_{do}	—	—	200	ns	+100pF
Address and Enable Outputs						
Turn ON Delay	t_{ad},t_{ed},t_{wd}	—	—	200	ns	1TTL Load
Turn OFF Delay	t_{eo}	—	—	100	ns	+100pF

All delays measured between 2.2 Volts and 0.7 Volts test points